IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A memory controller for use in a system having a program-addressable memory controlled by the memory controller and a processor coupled with the memory by an external bus, the memory controller comprising a compression map cache~~, said compression map cache~~ to store information that identifies a compressed cache line's worth of information stored in the memory, the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information ~~that has been compressed with another cache line's worth of information~~.

2. (Canceled)

3. (new) The memory controller of claim 1, wherein the information comprises a bit for each block of a plurality of blocks of memory space of the memory, wherein each of the plurality blocks stores its own cache line's worth of information, the bit to indicate whether its corresponding block is storing a compressed cache line's worth of information.

4. (new) The memory controller of claim 3, wherein the information further comprises an indication of the type of compression applied to the compressed cache line's worth of information when the bit indicates that its corresponding block is storing a compressed cache line's worth of information.

5. (new) The memory controller of claim 3, wherein, when all bits of the corresponding block is storing a same value, the value is identified in the information.

6. (new) The memory controller of claim 5, wherein the value is a value of 0.

7. (new) The memory controller of claim 1, wherein the information comprises a bit for each macro block of a plurality of macro blocks of memory space of the memory, where each macro block of memory space of the memory stores a cache lines' worth of information for a set of companion cache lines' worth of information, the bit to indicate whether the companion cache lines' worth of information of its corresponding macro block have been compressed.

8. (new) The memory controller of claim 7, wherein, when the bit indicates that the companion cache lines' worth of information of its corresponding macro block have been compressed, the information further comprises an indication of the type of compression applied to the companion cache lines' worth of information.

9. (new) The memory controller of claim 7, wherein, when all bits of the compressed companion cache lines' worth of information are storing a same value, the value is identified in the information.

10. (new) The memory controller of claim 9, wherein the value is a value of 0.

11. (new) The memory controller of claim 1 further comprising a memory space to identify physical continuous addressing space of the memory in which a compression map is stored.

12. (new) The memory controller of claim 11, wherein the memory space is to be written to by a computing system's BIOS.

13. (new) The memory controller of claim 1 further comprising a scheduler to schedule requests made to the memory controller, the scheduler coupled to the compression map cache to refer to the information to determine whether a request's corresponding cache line's worth of information is stored in the memory in a compressed state.

14. (new) The memory controller of claim 1 further comprising a first read path that flows through decompression logic circuitry and a second read path that bypasses the decompression logic circuitry, the decompression logic circuitry to decompress a compressed cache line's worth of information that has been read from the memory when

a request's corresponding cache line's worth of information is stored in memory in a compressed state.

15. (new) The memory controller of claim 1 further comprising compression logic circuitry coupled to a queue for queuing the requests, the compression logic circuitry to compress an uncompressed cache line's worth of information with a companion of the uncompressed cache line's worth of information.

16. (new) The memory controller of claim 15, wherein the compression logic circuitry is further coupled to a second queue for queuing responses to the requests.

17. (new) A processor and a memory controller integrated on a same semiconductor die, the memory controller controlling a program-addressable memory coupled with the processor by an external bus, the memory controller comprising a compression map cache to store information that identifies a compressed cache line's worth of information stored in the memory, the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information.

18. (new) The processor and memory controller of claim 17, wherein the information comprises a bit for each block of a plurality of blocks of memory space of the memory, each block of memory space of the memory to store its own cache line's worth of

information, the bit to indicate whether its corresponding block is storing a compressed cache line's worth of information.

19. (new) The processor and memory controller of claim 18, wherein, when the bit indicates that its corresponding block is storing a compressed cache line's worth of information, the information further comprises an indication of the type of compression applied to the compressed cache line's worth of information.

20. (new) The processor and memory controller of claim 18, wherein, when all bits of the corresponding block is storing a same value, the value is identified in the information.

21. (new) The processor and memory controller of claim 20, wherein the value is a value of 0.

22. (new) The processor and memory controller of claim 17, wherein the information comprises a bit for each macro block of a plurality of macro blocks of memory space of the memory, each macro block of memory space of the memory to store cache lines' worth of information for a set of companion cache lines' worth of information, the bit to indicate whether the companion cache lines' worth of information of its corresponding macro block have been compressed.

23. (new) The processor and memory controller of claim 22, wherein, when the bit indicates that the companion cache lines' worth of information of its corresponding

macro block have been compressed, the information further comprises an indication of the type of compression applied to the companion cache lines' worth of information.

24. (new) The processor and memory controller of claim 22, wherein, when all bits of the compressed companion cache lines' worth of information are storing a same value, the value is identified in the information.

25. (new) The processor and memory controller of claim 20, wherein the value is a value of 0.

26. (new) The processor and memory controller of claim 17 further comprising memory space to identify physical continuous addressing space of the memory in which a compression map is stored.

27. (new) The processor and memory controller of claim 26, wherein the memory space is to be written to by a computing system's BIOS.

28. (new) The processor and memory controller of claim 17 further comprising a scheduler to schedule requests made to the memory controller, the scheduler coupled to the compression map cache to refer to the information so that it can be understood whether a request's corresponding cache line's worth of information is stored in the memory in a compressed state.

29. (new) The processor and memory controller of claim 17 further comprising a first read path that flows through decompression logic circuitry and a second read path that bypasses the decompression logic circuitry, the decompression logic circuitry to decompress a compressed cache line's worth of information that has been read from the memory when a request's corresponding cache line's worth of information is stored in the memory in a compressed state.

30. (new) The processor and memory controller of claim 17 further comprising compression logic circuitry coupled to a queue for queuing the requests, the compression logic circuitry to compress an uncompressed cache line's worth of information with a companion of the uncompressed cache line's worth of information.

31. (new) The processor and memory controller of claim 30, wherein the compression logic circuitry is further coupled to a second queue for queuing responses to the requests.

32. (new) The processor and memory controller of claim 17, wherein the processor comprises a cache controller with compression logic circuitry, the compression logic circuitry to compress the first cache line's worth of information with the second cache line's worth of information to form the compressed cache line's worth of information.

33. (new) A computing system comprising:

a) a program-addressable memory; and

b) a processor and a memory controller integrated on a same semiconductor die, the memory controller controlling the memory, the memory controller comprising a compression map cache to store information that identifies a compressed cache line's worth of information stored in the memory, the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information.

34. (new) The computing system of claim 33, wherein the information comprises a bit for each block of a plurality of blocks of memory space within the memory, each block of memory space to store its own cache line's worth of information, the bit to indicate whether its corresponding block is storing a compressed cache line's worth of information.

35. (new) The computing system of claim 34, wherein, when the bit indicates that its corresponding block is storing a compressed cache line's worth of information, the information further comprises an indication of the type of compression applied to the compressed cache line's worth of information.

36. (new) The computing system of claim 34, wherein, when all bits of the corresponding block is storing a same value, the value is identified in the information.

37. (new) The computing system of claim 36, wherein the value is a value of 0.

38. (new) The computing system controller of claim 33, wherein the information comprises a bit for each macro block of a plurality of macro blocks of memory space within the memory, each macro block of memory space to store cache lines' worth of information for a set of companion cache lines' worth of information, the bit to indicate whether the companion cache lines' worth of information of its corresponding macro block have been compressed.

39. (new) The computing system of claim 38, wherein, when the bit indicates that the companion cache lines' worth of information of its corresponding macro block have been compressed, the information further comprises an indication of the type of compression applied to the companion cache lines' worth of information.

40. (new) The computing system of claim 38, wherein, when all bits of the compressed companion cache lines' worth of information are storing a same value, the value is identified in the information.

41. (new) The computing system of claim 36, wherein the value is a value of 0.

42. (new) The computing system of claim 33 further comprising memory space to identify physical continuous addressing space of the memory in which a compression map is stored.

43. (new) The computing system of claim 42, wherein the memory space is to be written to by the computing system's BIOS.

44. (new) A method by which a memory controller controlls a program-addressable memory coupled to a processor via an external bus:

snooping a cache that resides on the memory controller; and,

writing a cache line's worth of information into the memory, the snooping to gain access to information in the cache that pertains to the cache line's worth of information, the information to keep track of whether the cache line's worth of information is in a compressed state.

45. (new) The method of claim 44 further comprising the memory controller updating the information to reflect that the cache line's worth of information is compressed, the compressed cache line's worth of information received by the memory controller from the processor, the processor having compressed companion uncompressed cache lines' worth of information to form the compressed cache line's worth of information.

46. (new) The method of claim 45 further comprising the processor identifying the compressed cache line's worth of information as being in a compressed state.

47. (new) The method of claim 46, wherein identifying the compressed cache line's worth of information as being in a compressed state further comprises configuring header information associated with the compressed cache line's worth of information.

48. (new) The method of claim 44 further comprising the memory controller updating the information to reflect that the cache line's worth of information is uncompressed, the uncompressed cache line's worth of information received by the memory controller from the processor, the processor having decompressed a compressed cache lines' worth of information to form the uncompressed cache line's worth of information.

49. (new) The method of claim 48 further comprising the processor identifying the uncompressed cache line's worth of information as being in a compressed state.

50. (new) The method of claim 49, wherein identifying the uncompressed cache line's worth of information as being in a compressed state further comprises setting a bit in header information associated with the uncompressed cache line's worth of information.

51. (new) The method of claim 44 further comprising the memory controller receiving a second cache line's worth of information in an uncompressed state, the second cache line's worth of information received by the processor that does not posses compression logic circuitry.

52. (new) The method of claim 51 further comprising the memory controller recognizing within the memory controller a third cache line's worth of information that is in an uncompressed state and is a companion to the second cache line's worth of information, and, the memory controller compressing the second and third cache lines'

worth of information to form the cache line's worth of information, the memory controller updating the information to reflect that the cache line's worth of information is in a compressed state.

53. (new) The method of claim 44 further comprising the memory controller receiving the cache line's worth of information in an uncompressed state, the cache line's worth of information received by a processor that does not posses compression logic circuitry, the memory controller recognizing within the memory controller a second cache line's worth of information that is in an uncompressed state and is a companion to the cache line's worth of information, and, the memory controller not compressing the cache line's worth of information with the second cache lines' worth of information because the memory controller deems them uncompressible, the memory controller updating the information to reflect that the cache line's worth of information is in an uncompressed state.

54. (new) The method of claim 44 further comprising fetching the information from the memory if the snooping misses.

55. (new) The method of claim 44 further comprising writing the cache line's worth of information into half of a macro block if the cache line's worth of information is in a compressed state.

56. (new) The methodology of claim 44 further comprising writing the cache line's worth of information into both halves of a macro block if the cache line's worth of information is in a compressed state

57. (new) A method, comprising

by a memory controller that controls a program-addressable memory coupled with a processor by an external bus:

snooping a cache that resides on the memory controller; and,

reading a cache line's worth of information from the memory, the snooping to gain access to information in the cache that pertains to the cache line's worth of information, the information to keep track of whether the cache line's worth of information is in a compressed state.

58. (new) The method of claim 57 further comprising the memory controller decompressing the cache line's worth of information if the information indicates that the cache line's worth of information is in a compressed state.

59. (new) The method of claim 58 further comprising the memory controller sending the cache line's worth of information to the processor, wherein the processor does not posses decompression logic circuitry.

60. (new) The method of claim 57 further comprising the memory controller receiving a request for a second cache line's worth of information that is a companion to a first cache

line's worth of information, where, an earlier received request for the first cache line's worth of information caused the reading, the method further comprising the memory controller not performing a read of the memory to satisfy the request for the second cache line's worth of information because the information indicates that the cache line's worth of information is in a compressed state.

61. (new) The method of claim 57, wherein the cache line's worth of information is in a compressed state, the reading further comprising reading the cache line's worth of information from a different half of a macro block than the cache line's worth of information would have been read from by the memory controller if it were in an uncompressed state, the reading from a different half a consequence of the information indicating that the cache line's worth of information is in a compressed state.

62. (new) The method of claim 57 further comprising the memory controller not decompressing the cache line's worth of information because the information indicates that the cache line's worth of information is in an uncompressed state.

63. (new) The method of claim 62 further comprising the memory controller sending the cache line's worth of information to the processor, wherein the processor does not posses decompression logic circuitry.

64. (new) The method of claim 57 further comprising the memory controller receiving a request for a second cache line's worth of information that is a companion to a first cache

line's worth of information, where, an earlier received request for the first cache line's worth of information caused the reading, the method further comprising the memory controller performing a read of the memory to satisfy the request for the second cache line's worth of information because the information indicates that the cache line's worth of information is in an uncompressed state.

65. (new) The method of claim 57 further comprising the memory controller fetching the information from the memory because the snooping missed.

66. (new) The method of claim 65 where the memory controller services requests by accessing the memory in a pipelined fashion, the reading to service a second request, the method further comprising the memory controller performing at least portions of the snooping and the fetching while the memory controller operates to read another cache line's worth of information from the memory to service an earlier received first request.

67. (new) The method of claim 65 further comprising the memory controller predicting a compressed or uncompressed state for the cache line's worth of information after the cache miss, and, the reading further comprising reading the cache line's worth of information from a macro block half in accordance with the predicting, the fetching not being completed prior to the starting of the reading.

68. (new) The method of claim 67 further comprising validating the accuracy of the prediction after the fetching is completed.